

VK-RZ/A1LU

ver. 2.2

R7S721030VCFP

- 384MHz, 176 QFP, Fanless

3 MByte OnChip RAM

- Can RUN without ext. SDRAM

Up to 64 MByte NOR-Flash / 16 MB on board

- QSPI, 64MHz, Quad (Burst), 4-bit
- Direct fetch is possible

Up to 64 MByte SDRAM / 32 MB on board

- 64MHz, 16-bit

1 x USB Function

- USB 2.0, Micro USB connector

Micro SD

- SDHI1

User interface

- LED
- Push button

CMOS camera interface

- KBCR-M04VG-HPB2033VGA 640x480, up to 60fps, horizontal angle 98 degrees, vertical angle 75 degrees

Audio codec MAX9867ETJ+

- 3.5mm , 4 pole audio input / output jack

Wi-Fi / BLE

- Pre certified ESP32 wireless module

Exp. Ports

- RZ/A1LU - 14 I/O 3.3V
- UART
- SPI
- I2C
- ADC

Debug ports:

- RZ/A1 J-TAG 2x5 pins, Coresight™

DC IN +5V

- Consumption 250mA max

Operating temperature:

- -40 ... +85°

Dimensions:

- 45 mm x 45 mm
- Mounting holes 4 x Ø2 mm (40 mm x 40mm)

Embedded camera to USB/Wi-Fi/BLE
small form factor module with
Renesas Electronics RZ/A1LU ARM Cortex-A9 LSI



Planned Board Support Packages:

- H.264 video encoding
- H.264/MJPEG IP camera over RTSP/RTP
- UVC 1.0 compliant USB 2.0 camera supporting YUV, MJPEG, H.264
- MBED enabled
- u-boot, Linux - GCC
- FreeRTOS - IAR
- OpenCV V3.2
- IS2T MicroEJ demos - IAR
- .NET Micro Framework - GCC



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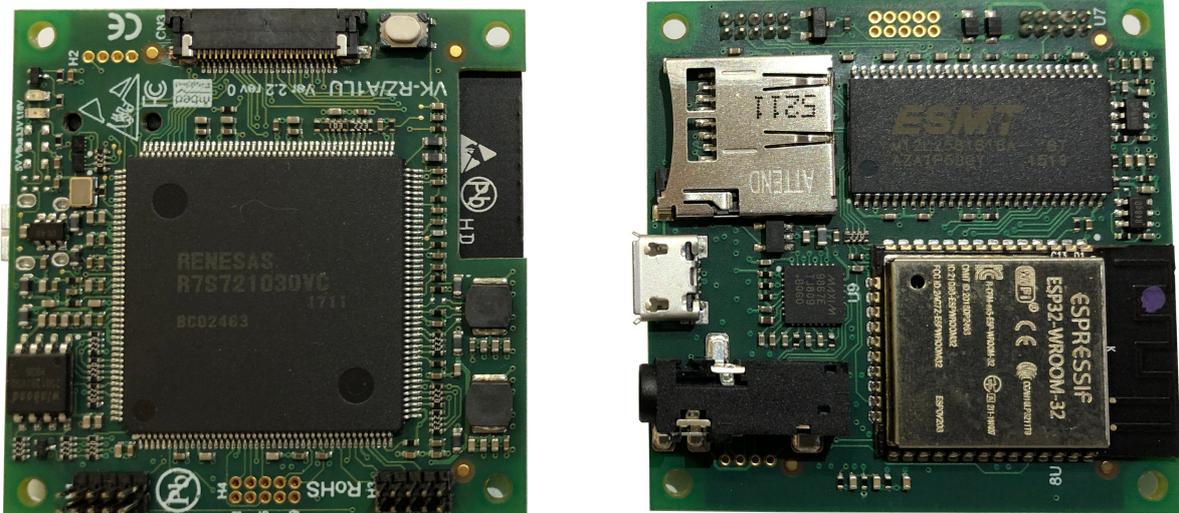
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1. Introduction

VK-RZ/A1LU is a starter kit, equipped with R7S721030VCFP MCU from Renesas Electronics. This powerful LSI single-chip microcontroller includes an ARM Cortex™-A9 processor along with the integrated peripheral functions required to configure a system.



VK-RZ/A1LU board (Top & Bottom view)

The core includes:

- ✓ 32-KB L1 instruction cache, 32-KB L1 data cache
- ✓ 128-KB L2 cache



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Integrated various on-chip peripheral functions and interfaces such as:

- ✓ 3-MB large-capacity RAM (128 KB are shared by the data-retention RAM).
- ✓ Data-retention RAM
- ✓ Multi-function timer pulse unit 2, OS timer, Realtime clock
- ✓ UART, UART with FIFO, I²C, SPI, SPI multi I/O bus controller, CAN
- ✓ I²S, SPDIF
- ✓ A/D converter, SCUX
- ✓ SD host interface, MMC host interface
- ✓ Ethernet controller, Ethernet AVB
- ✓ USB 2.0 (host/functions)
- ✓ video display controller 5
- ✓ JPEG codec unit, Capture engine unit
- ✓ Interrupt controller modules, General I/O ports

Kit supports:

- ✓ WiFi/BLE connectivity
- ✓ CMOS camera input
- ✓ up to 64 MB QSPI FLASH
- ✓ up to 64 MB SDRAM
- ✓ Micro SD cards
- ✓ Micro USB 2.0
- ✓ Stereo audio output & mono input
- ✓ 1 push button
- ✓ JTAG interface

All this along with DC/DC power supply on board and pin headers with unused pins of RZ/A1LU allows you to build a diversity of powerful applications which can be used in a wide range of embedded tasks.



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2. Board Features

- ✓ LSI: RZ/ALU (R7S721030VCFP)
 - Power supply voltage: V_{DD} 3.0 ÷ 3.6 V
 - Operating ambient temperature: T_A -40 ÷ +85 °C
 - Max CPU clock: $I\phi$ 400 MHz
- ✓ Micro USB (B type connector ↔ USB[function] ↔ RZ/ALU[device])
- ✓ 16 MB FLASH (Winbond 25Q128JVSQ ↔ QSPI ↔ RZ/ALU)
- ✓ 32 MB SDRAM (ESMT M12L2561616A-6T ↔ RZ/ALU)
- ✓ Micro SD card connector (RZ/ALU)
- ✓ WiFi module (Espressif ESP32 WROOM32 ↔ UART/SPI ↔ RZ/ALU)
- ✓ Audio codec (4 pin 3.5 mm jack ↔ MAX9867ETJ ↔ I²S ↔ RZ/ALU)
- ✓ CMOS camera interface (KBCR-M04VG-HPB2033VGA ↔ DV0[8bit] ↔ RZ/ALU)
- ✓ User Button (↔ RZ/ALU)
- ✓ JTAG debug/programing interface (10 pin connector ↔ RZ/ALU)
- ✓ FR-4, 1.6 mm, 6 Layers, Green solder mask, White component print
- ✓ Dimensions: 45.0 mm x 45.0 mm (Holes: 4x 2 mm, between centers: 40 mm)

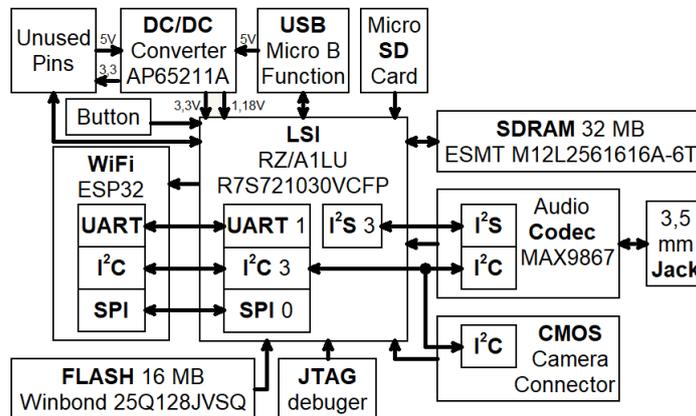
3. Electrostatic WARNING

VK-RZ/A1LU board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.



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4. Block Diagram



5. External SDRAM

CS3: ORIGIN = **0x0C000000** LENGTH = **64 MB**

CS3 mirror ORIGIN = **0x4C000000** LENGTH = **64 MB**

!!! SDRAM chip is accessed with 16bit data width !!!

6. Power supply

VK-RZ/A1LU is powered by **5 V** DC. The voltage can come either from external header or USB Micro B connector. Consumption of the board may vary and the maximum is **250 mA**.

7. Clock Circuits

Quartz Generator 48.0000 MHz is connected to **USB_X1**, pin# **139** of **RZ/A1LU**

USB_X1/2 (CLK-CAM) 24.0000 MHz is connected to **XCik**, pin# **13** of **CN2**

USB_X1/4 (CLK-AUD) 12 MHz is connected to **AUDIO_X1**, pin# **91** of **RZ/A1LU**

USB_X1/4 (CLK-Codec) 12 MHz is connected to **MCik**, pin# **31** of **MAX9867**



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8. Push button

SB1			
Pin #	Name	Signal Name	Tied to pin #
1	-	P1_12	82 (RZ/A1LU)
2	-	GND	-

9. External connectors

9.1 USB & Power

CN1			
Pin #	Name	Signal Name	Tied to pin #
1	+5V	VBUS	152 (RZ/A1LU)
2	D-	DM0	150 (RZ/A1LU)
3	D+	DP0	151 (RZ/A1LU)
4	ID	NC	-
5	G	GND	-

9.2 JTAG

H1			
Pin #	Name	Signal Name	Tied to pin #
1	VREF	3.3V	-
2	TMS	JTAG-TMS	100 (RZ/A1LU)
3	GND	GND	-
4	TCK	JTAG-CLK	101 (RZ/A1LU)
5	GND	GND	-
6	TDO	JTAG-TDO	98 (RZ/A1LU)
7	GND	GND	-
8	TDI	JTAG-TDI	99 (RZ/A1LU)
9	GND	GND	-
10	RESET	$\overline{\text{RZRST}}$	76 (RZ/A1LU)



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9.3 WiFi Module

ESP32 - WROOM - 32			
Pin #	Name	Signal Name	Tide to pin #
1	g	GND	-
2	3V3	3.3V	-
3	EN	ESP_EN	135 (RZ/A1LU)
4	Sensor VP	NC	-
5	Sensor VN	NC	-
6	IO34	NC	-
7	IO35	NC	-
8	IO32	NC	-
9	IO33	NC	-
10	IO25	SCL3	131 (RZ/A1LU)
11	IO26	SDA3	132 (RZ/A1LU)
12	IO27	NC	-
13	IO14	SCLK0	17 (RZ/A1LU)
14	IO12	MISO0	22 (RZ/A1LU)
15	g	GND	-
16	IO13	MOSI0	20 (RZ/A1LU)
17	SD2	NC	-
18	SD3	NC	-
19	CMD	NC	-
20	CLK	NC	-
21	SD0	NC	-
22	SD1	NC	-
23	IO15	SSL0	19 (RZ/A1LU)
24	IO2	ESP_IO2	137 (RZ/A1LU)
25	IO0	ESP_IO0	136 (RZ/A1LU)
26	IO4	NC	-
27	IO16	NC	-
28	IO17	NC	-
29	IO5	NC	-
30	IO18	NC	-
31	IO19	RTS1	165 (RZ/A1LU)
32	NC	NC	-
33	IO21	NC	-
34	RXD0	TxD1	133 (RZ/A1LU)
35	TXD0	RxD1	65 (RZ/A1LU)
36	IO22	CTS1	164 (RZ/A1LU)
37	IO23	NC	-
38	g	GND	-
39	g	GND	-



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9.4 Micro SD card slot

CN3			
Pin #	Name	Signal Name	Tied to pin #
1	DAT2	SDC-D2	51 (RZ/A1LU)
2	CD/DAT3	SDC-D3	49 (RZ/A1LU)
3	CMD	SD-CMD	48 (RZ/A1LU)
4	Vdd	3.3V	-
5	CLK	SDC-CLK	47 (RZ/A1LU)
6	Vss	GND	-
7	DAT0	SDC-D0	45 (RZ/A1LU)
8	DAT1	SDC-D1	44 (RZ/A1LU)
9	S1	NC	-
10	G1	GND	-
11	S2	-	External logic
12	G2	GND	-
13	Gnd	GND	-
14	Gnd	GND	-

9.5 Audio Jack

J1			
Pin #	Name	Signal Name	Tied to pin #
1	JACKSNS	Mic	17 (MAX9867)
2	LOutP	Left	22 (MAX9867)
3	ROutP	Right	19 (MAX9867)
4	LOutN	Common	21 (MAX9867)



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9.6 CMOS Camera input

CN2			
Pin #	Name	Signal Name	Tied to pin #
1	SFin	-	-
2	AGND	GND	-
3	SIOD	SDA3	132 (RZ/A1LU)
4	AVdd	3.3V	-
5	SIOC	SCL3	131 (RZ/A1LU)
6	Reset	CAM_RSTB	55 (RZ/A1LU)
7	VSYNC	DV0-VSYNC	53 (RZ/A1LU)
8	PWDN	CAM-PWDN	33 (RZ/A1LU)
9	HREF	DV0-HSYNC	54 (RZ/A1LU)
10	VCore	NC	-
11	DVdd	3.3V	-
12	Y9	DV0-DATA7	81 (RZ/A1LU)
13	XClk	CLK-CAM	-
14	Y8	DV0-DATA6	80 (RZ/A1LU)
15	DGND	GND	-
16	Y7	DV0-DATA5	79 (RZ/A1LU)
17	PClk	DV0-CLK	52 (RZ/A1LU)
18	Y6	DV0-DATA4	78 (RZ/A1LU)
19	Y2	DV0-DATA0	125 (RZ/A1LU)
20	Y5	DV0-DATA3	128 (RZ/A1LU)
21	Y3	DV0-DATA1	126 (RZ/A1LU)
22	Y4	DV0-DATA2	127 (RZ/A1LU)
23	Y1	NC	-
24	Y0	NC	-



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10. Unused Pin Headers

H3	
Pin #	Functions
1	3.3V
2	P6-12/D28/LCD0_DATA20/SCLK1/SSISCK2/ $\overline{\text{RTS0}}$ /DV0_DATA0
3	3.3V
4	P6-13/D29/LCD0_DATA21/SSL10/SSIWS2/ $\overline{\text{CTS0}}$ /DV0_DATA1
5	5V
6	P6-14/D30/LCD0_DATA22/MOSI1/SSIDATA2/RxD0/DV0_DATA2
7	5V
8	P6-15/D31/LCD0_DATA23/MISO1/TxD0/DV0_DATA3
9	GND
10	GND

H4	
Pin #	Functions
1	P1-4/SCL2/IRQ0/DREQ0/VIO_D0
2	P6-1/D17/LCD0_DATA9/SSL00/TCLKB
3	P1-5/SDA2/IRQ1/VIO_D1
4	P6-2/D18/LCD0_DATA10/MOSI0/TCLKC
5	P6-0/D16/LCD0_DATA8/SCLK0/TCLKA/WDTOVF
6	P6-3/D19/LCD0_DATA11/MISO0/TCLKD
7	P1-13/AN5/IRQ5/ET_RXD1/VIO_D5
8	P6-9/D25/LCD0_DATA17/SSIWS0/IRQ2/TIOC3C/TRACED_ATA2
9	P1-14/AN6/IRQ6/ET_RXD2/VIO_D6
10	P6-10/D26/LCD0_DATA18/SSITxD0/IRQ3/TIOC3D/CAN1TX/ TRACED_ATA3



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11. Available Demo Software

11.1 Audio Wave Demo

This Demo reads *.wav files from SD card and plays them through the **MAX9867** stereo audio codec. When you press the button, you can skip currently played song and next found in SD card will be played. You will need a headphones to hear the songs.

11.2 UVC JPEG Demo

This Demo turns VK-RZ/A1LU board in to a standard USB Camera. Every USB host which supports the standard **UVC** protocol (v1.0), should be able to get the stream and play it. The format of the stream is **MJPEG** and supported resolution is 640 x 480 @ 30 fps.

Here are some examples how to grab the stream from the USB:

➤ Using VLC as a player:

Go to: "Media" → "Open Capture Device..."

for "Video device name" select: **UVC**, for "Audio device name" select: **None**

Press **Play**.

➤ Using FFMPEG as a player:

Open a CMD/BASH terminal

Insert: `ffmpeg -f dshow -i video="UVC" / ffplay -i /dev/video0`

A window will be opened and you will be able to see the stream.

11.3 x264/MJPEG WiFi Streaming Demo

This Demo turns VK-RZ/A1LU board in to standalone RTSP server. On startup this demo waits SD card and looks for a file `STARTUP.json`. It contains WiFi Access Point's credential information. After the file is found, the board connects to the specific AP's SSID, creates RTSP server & waits for a client. This state is indicated with a continuous lighting of LED1. Currently only 1 client can be connected to the server. If you want to change credential information or the stream format, you should alter the `STARTUP.json` file.

Second variant of this demo is available, which takes advantage of the ESP's SPI bus. The actual communication channel [MCU <-> ESP32] becomes faster & allows higher fps rate in MJPEG format. The rate in x264 format, remains intact.



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```
{
  "CFG": {
    "WIFI_SSID":      "VT",
    "WIFI_PASSWORD": "vekatech1560",
    "STREAM_TARGET": "192.168.2.123",
    "STREAM_FORMAT": "X264",
    "STREAM_STATUS": "YES"
  }
}
```

STARTUP.json listing

STREAM_FORMAT parameter can be either **X264** or **MJPEG**

- For X264 supported resolution is 320 x 240 @ 15 fps
- For MJPEG supported resolution is 320 x 240 @ 5 fps (UART) / 15 fps (SPI).

STREAM_TARGET is used as destination IP when RTP is used **alone**, but when RTSP is used, this parameter is ignored.

STREAM_STATUS parameter can be either **YES** or **NO**. It enables or disables logging of statistics information on UART 0. (Header H3) This information is actually the generated network traffic by the RTP/RTSP server. (you will need USB serial adapter to see this information).

Here are some examples how to grab the stream from the RTSP server:

- Using VLC as a player:

Go to: "Media" → "Open Network Stream..."

for "URL" enter this: `rtsp://VK_RZ_A1LU's_IP:554/Cam`

Check "Show more options" & in "Edit Options" add this: `:ipv4-timeout=20000`

Press Play.

- Using FFmpeg as a player:

Open a CMD/BASH terminal

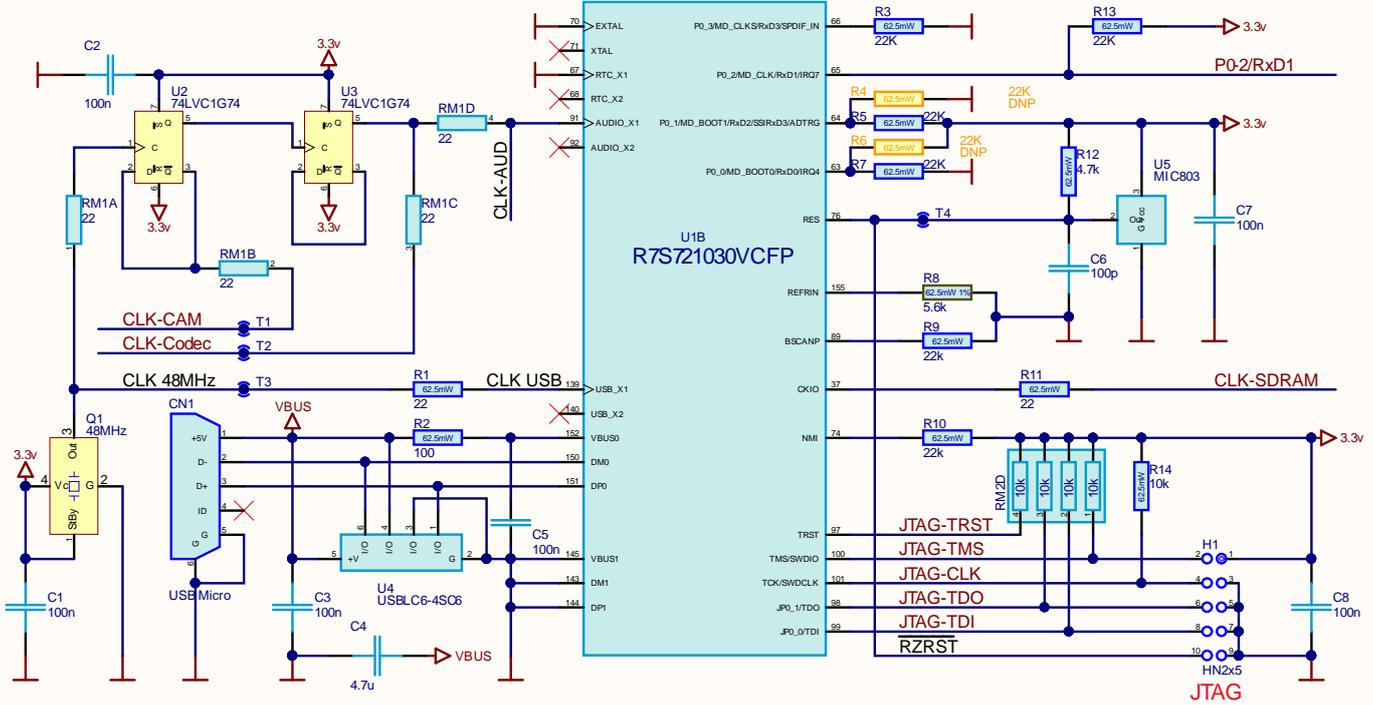
Insert: `ffmpeg rtsp://VK_RZ_A1LU's_IP:554/Cam`

A window will be opened and you will be able to see the stream.



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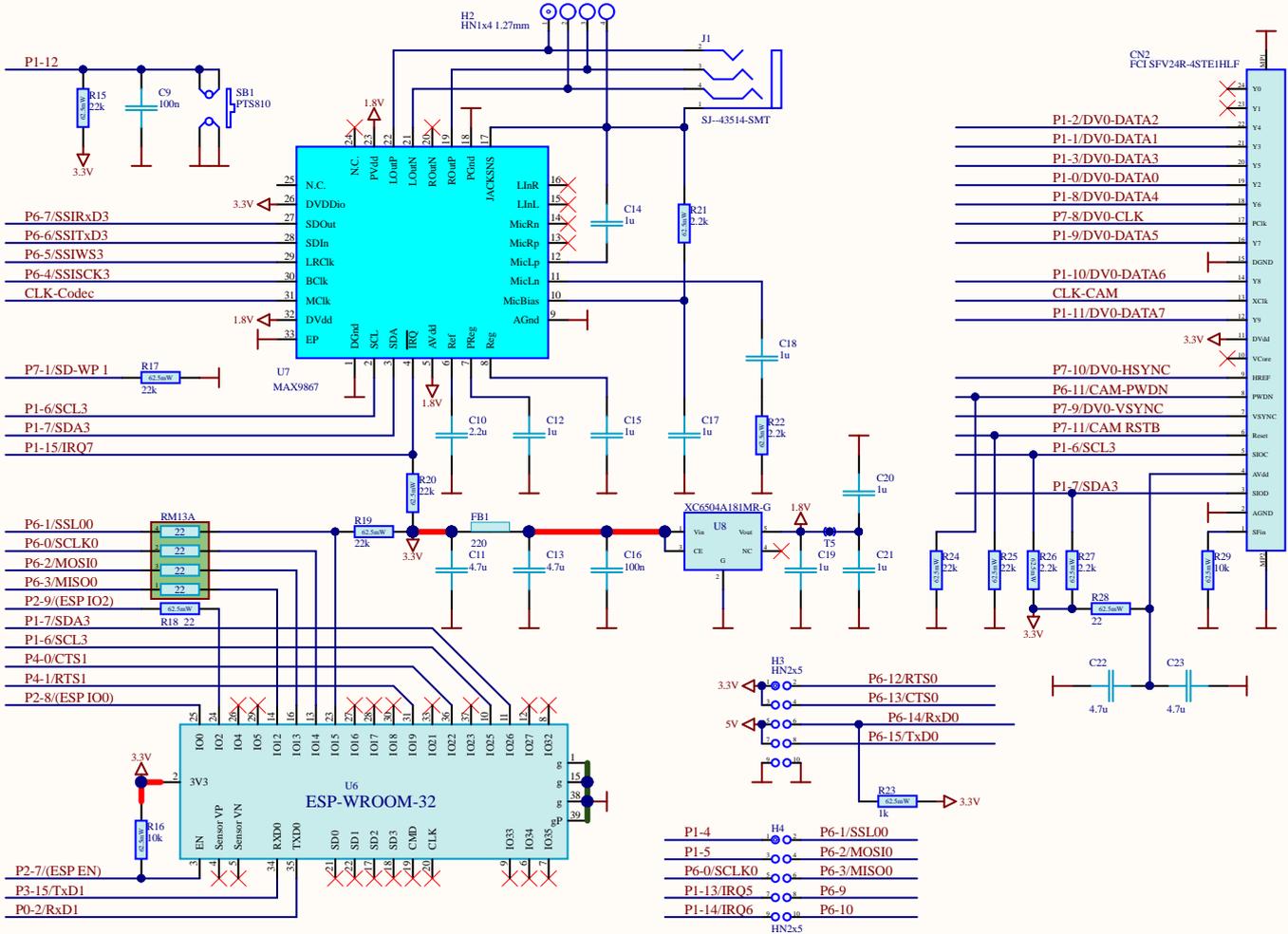
12. Schematics



U1A		R7S721030VCFP	
P1-0/DV0-DATA0	125	P1_0_R1RC0SCLRQ4/ET_RXD0/DV0_DATA0	
P1-1/DV0-DATA1	126	P1_1_R1RC0SDA1RQ05/ET_RXD1/DV0_DATA1	
P1-2/DV0-DATA2	127	P1_2_R1RC1SCLRQ6/ET_RXD2/DV0_DATA2	
P1-3/DV0-DATA3	128	P1_3_R1RC1SDA1RQ7/ET_RXD3/DV0_DATA3	
P1-4	129	P1_4_R1RC2SCLRQ0/DREQ0/VIO_D0	
P1-5	130	P1_5_R1RC2SDA1RQ1/VIO_D1	
P1-6/SCL3	131	P1_6_R1RC3SCLRQ2/SSIR-d0/VIO_D2	
P1-7/SDA3	132	P1_7_R1RC3SDA1RQ3/Rd2/VIO_D3	
P1-8/DV0-DATA4	78	P1_8_AN0IRQ0/Rd0/DV0_DATA4	
P1-9/DV0-DATA5	79	P1_9_AN1IRQ1/Rd1/DV0_DATA5	
P1-10/DV0-DATA6	80	P1_10_AN2IRQ2/Rd2/DV0_DATA6	
P1-11/DV0-DATA7	81	P1_11_AN3IRQ3/Rd3/DV0_DATA7	
P1-12	82	P1_12_AN4IRQ4/ET_RXD0/VIO_D4	
P1-13/IRQ5	83	P1_13_AN5IRQ5/ET_RXD1/VIO_D5	
P1-14/IRQ6	84	P1_14_AN6IRQ6/ET_RXD2/VIO_D6	
P1-15/IRQ7	85	P1_15_AN7IRQ7/ET_RXD3/VIO_D7	
P2-0/CS3	56	P2_0_CS3_R1LN3RX/SPDIF_IN/RQ7	
P2-1/RAS	57	P2_1_RAS_R1LN3TX/SPDIF_OUT/RQ6	
P2-2/CAS	58	P2_2_CAS_CANIRX/TIOC0B/IRQ5	
P2-3/CKE	60	P2_3_CKE_CANITX/TIOC0D	
P2-4/DQMLL	94	P2_4_WED0/DQMLL/TIOC4A	
P2-5/DQMLU	96	P2_5_WEU1/WED0/DQMLU/TIOC3A	
P2-6/RD/WR	134	P2_6_RD/WR/SIRd3/TIOC2A	
P2-7/(ESP EN)	135	P2_7_CS0/SSISCK1/TIOC1A/IRQ2	
P2-8/(ESP IO0)	136	P2_8_RD/SSITd3/TIOC1A/CANITX	
P2-9/(ESP IO2)	137	P2_9_A0/SSWS3/SCK0/IRQ1/CANIRX	
P3-0/A1/SD-D2 0	103	P3_0_A1/SD_D2_0/LCD0_DATA0/ET_TXCLK	
P3-1/A2/SD-D3 0	104	P3_1_A2/SD_D3_0/LCD0_DATA1/ET_TXNR	
P3-2/A3/SD-CMD 0	106	P3_2_A3/SD_CMD_0/LCD0_DATA2/ET_TXEN	
P3-3/A4/SD-CLK 0	108	P3_3_A4/SD_CLK_0/LCD0_DATA3/ET_RXCLK	
P3-4/A5/SD-D0 0	110	P3_4_A5/SD_D0_0/LCD0_DATA4/ET_RXNR	
P3-5/A6/SD-D1 0	111	P3_5_A6/SD_D1_0/LCD0_DATA5/ET_RXDV	
P3-6/A7/SD-WP 0	112	P3_6_A7/SD_WP_0/LCD0_DATA6/ET_COL	
P3-7/A8/SD-CD 0	113	P3_7_A8/SD_CD_0/LCD0_DATA7/ET_CRS	
P3-8/A9	114	P3_8_A9/AUD0_CLK/DV0_DATA8/SCK3	
P3-9/A10	115	P3_9_A10/SPDIF_OUT/DV0_DATA9/ET_D3	
P3-10/A11	117	P3_10_A11/SPBIO1_0/TIOC3B/DV0_DATA10/Rd3	
P3-11/A12	118	P3_11_A12/SPBIO1_0/TIOC3C/DV0_DATA11	
P3-12/A13	120	P3_12_A13/SPBIO2_0/TIOC3D/DV0_DATA12	
P3-13/A14	122	P3_13_A14/SPBIO3_0/TIOC3E/DV0_DATA13	
P3-14/A15	124	P3_14_A15/VIO_CLK/SPDIF_IN/DV0_DATA14/SCK1/AUD0_XOUT2	
P3-15/TXD1	133	P3_15_A16/VIO_FLD/DV0_DATA15/Td1	
P4-0/CTS1	164	P4_0_A17/VIO_VD/TIOC1B/ET_MDC/CTS1	
P4-1/RTS1	165	P4_1_A18/VIO_HD/TIOC2B/ET_MDIO/RTS1	
P4-2/SPBIO20-0	166	P4_2_A19/SPBIO20_0/TRACEDATA2	
P4-3/SPBIO30-0	167	P4_3_A20/SPBIO30_0/TRACEDATA3	
P4-4/SPBCLK-0	168	P4_4_A21/SPBCLK_0/TRACECLK	
P4-5/SPBSSL-0	169	P4_5_A22/SPBSSL_0/TRACECTL	
P4-6/SPBIO00-0	170	P4_6_A23/SPBIO00_0/TRACEDATA0	
P4-7/SPBIO10-0	172	P4_7_A24/SPBIO10_0/TRACEDATA1	
P5_0/D0	173	P5_0_D0/MMC_D4/ET_TXD0/DV0_DATA16/LCD0_TC0N0	
P5-1/D1	175	P5_1_D1/MMC_D5/ET_TXD1/DV0_DATA17/LCD0_TC0N1	
P5-2/D2	176	P5_2_D2/MMC_D6/ET_TXD2/DV0_DATA18/LCD0_TC0N2	
P5-3/D3	1	P5_3_D3/MMC_D7/ET_TXD3/DV0_DATA19/LCD0_TC0N3	
P5-4/D4	2	P5_4_D4/RSPCK2/SISCK1/DV0_DATA20	
P5-5/D5	3	P5_5_D5/SSL20/SSWS1/DV0_DATA21	
P5-6/D6	4	P5_6_D6/MOS0/SSITd1/DV0_DATA22/SCK2	
P5-7/D7	5	P5_7_D7/MISO2/SSIRd1/DV0_DATA23/Td2	
P5-8/D8	6	P5_8_D8/CAN0RX/TIOC4A/IRQ3	
P5-9/D9	8	P5_9_D9/CAN0TX/TIOC4B/IRQ4	
P5-10/D10	10	P5_10_D10/IRd0/TIOC4C/IRQ5	
P5-11/D11	12	P5_11_D11/IRd1/TIOC4D/IRQ6	
P5-12/D12	13	P5_12_D12/SSISCK2/SCK4/AUD0_XOUT2	
P5-13/D13	14	P5_13_D13/SSWS2/AUD0_XOUT/AUD0_XOUT3	
P5-14/D14	15	P5_14_D14/SSIDATA2/Rd4/DV0_DATA24	
P5-15/D15	16	P5_15_D15/SD_WP_1/Td4	
P6-0/SCLK0	17	P6_0_D16/LCD0_DATA18/RSPCK0/TCLKA/WDT0FP	
P6-1/SSL0	19	P6_1_D17/LCD0_DATA19/SSL0/TCLKB	
P6-2/MOSI0	20	P6_2_D18/LCD0_DATA20/MOSI0/TCLKC	
P6-3/MISO0	22	P6_3_D19/LCD0_DATA21/MISO0/TCLKD	
P6-4/SSISCK3	24	P6_4_D20/LCD0_DATA22/SSISCK3/MLB_CLK	
P6-5/SSISWS3	26	P6_5_D21/LCD0_DATA23/SSISWS3/MLB_SIG	
P6-6/SSITxD3	27	P6_6_D22/LCD0_DATA24/SSITd3/MLB_DAT	
P6-7/SSIRxD3	28	P6_7_D23/LCD0_DATA25/SSIRd3/IRQ0/TIOC3A_RLN3RX	
P6-8/LED	29	P6_8_D24/LCD0_DATA26/SSISCK0/IRQ1/TIOC3B_RLN3RXT	
P6-9	30	P6_9_D25/LCD0_DATA27/SSISWS0/IRQ2/TIOC3C	
P6-10	32	P6_10_D26/LCD0_DATA28/SSITd0/IRQ3/TIOC3D/CANITX	
P6-11/CAM-PWDN	33	P6_11_D27/LCD0_DATA29/SSIRd0/SSIDATA2/SCK0/CANIRX	
P6-12/RTS0	35	P6_12_D28/LCD0_DATA30/RSPCK1/SISCK3/RTS0/DV0_DATA40	
P6-13/CTS0	38	P6_13_D29/LCD0_DATA31/SSL10/SSISWS3/CTS0/DV0_DATA41	
P6-14/RxD0	40	P6_14_D30/LCD0_DATA32/MOSI1/SSIDATA2/Rd0/DV0_DATA42	
P6-15/TxD0	41	P6_15_D31/LCD0_DATA33/MISO1/Td0/DV0_DATA43	
P7-0/SD-CD 1	42	P7_0_LCD0_EXTCLK/MMC_CD/SD_CD_1/SPDIF_OUT/TIOC2A/DV0_DATA44/SCK3/SCK0	
P7-1/SD-WP 1	43	P7_1_CS1/AUD0_XOUT3/WP_1/Td2/DV0_DATA45/SCL_RSD0/Rd4	
P7-2/SD-D1 1	44	P7_2_CS4/MMC_D1/SD_D1_1/IRQ/CAN0RX/DV0_DATA46/SCL_TXD0/Rd3	
P7-3/SD-D0 1	45	P7_3_CS5/MMC_D0/SD_D0_1/IRQ/CAN0TX/DV0_DATA47/SCL_CTS0/RTS0	
P7-4/SD-CLK 1	47	P7_4_WAIT/MMC_CLK/SD_CLK_1/IRd0/LCD0_CLK/SCL/SCK1	
P7-5/SD-CMD 1	48	P7_5_BS/MMC_CMD/SD_CMD_1/Td0/IRd0/LCD0_TC0N4/SCL/Rd1	
P7-6/SD-D3 1	49	P7_6_WED0/MUL/MMC_D3/SD_D3_1/IRQ6/CTS2/LCD0_TC0N5/SCL/TXD1	
P7-7/SD-D2 1	51	P7_7_WED0/MUL/AH/MMC_D2/SD_D2_1/IRQ5/RIS2/LCD0_TC0N6/SCL/CTS1/RIS1	
P7-8/DV0-CLK	52	P7_8_CS2/SSISCK1/DV0_CLK/IRQ3/Td0	
P7-9/DV0-VSYNC	53	P7_9_A25/SSWS1/DV0_VSYNC/IRQ5/SCK3/TIOC1A	
P7-10/DV0-HSYNC	54	P7_10_TEND0/SSITd1/DV0_HSYNC/Rd3	
P7-11/CAM RSTB	55	P7_11_DACK0/SSIRd1/CAN_CLK/SCK2/Td3/AUD0_XOUT/AUD0_XOUT3	



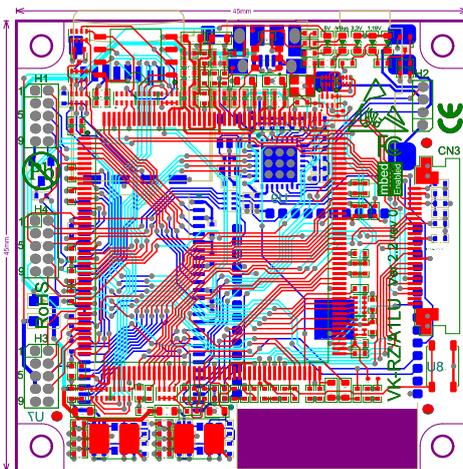
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13. PCB

CONSTRAINTS
 Min Trace/Gap ----- 0,15 mm
 Min Drill Hole Diameter ---- 0,2 mm
 Min Annular Ring ----- 0,15 mm
 LPI Color ----- Mat green
 Finished Copper Weight --- 1 oz
 Surface finish Immersion --- Gold

Top Layer
 Signal Layer 1
 Bottom Layer

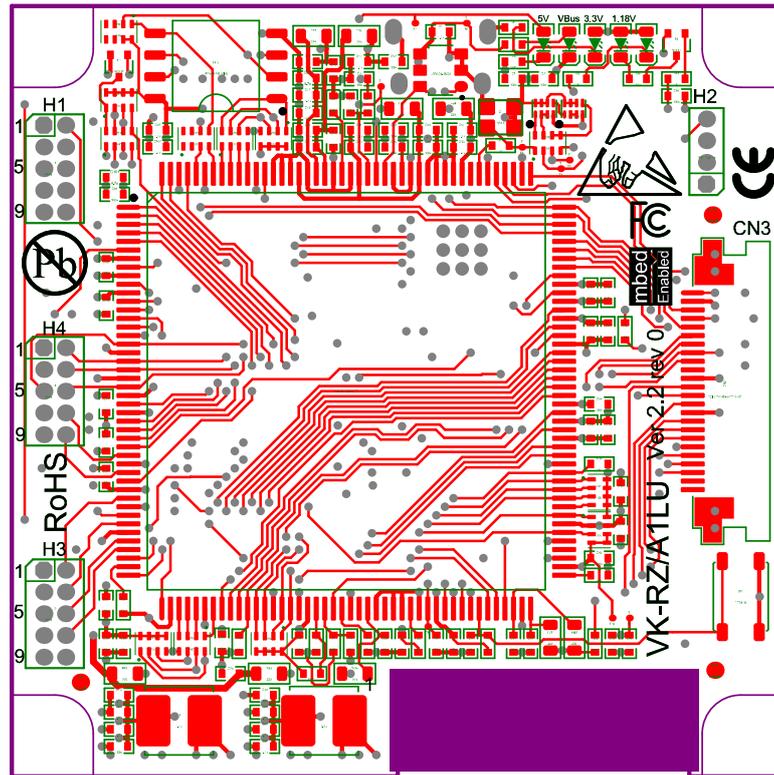


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,010mm	3,5	
3	Top Layer	Copper	0,035mm		
4	Dielectric 1	FR-4	0,254mm	4,2	
5	Signal Layer 1	Copper	0,035mm		
6	Dielectric 4		0,254mm	4,2	
7	1,18V	Copper	0,035mm		
8	Dielectric 2		0,254mm	4,2	
9	3,3V	Copper	0,035mm		
10	Dielectric 6		0,254mm	4,2	
11	Gnd	Copper	0,035mm		
12	Dielectric 5		0,254mm	4,2	
13	Bottom Layer	Copper	0,035mm		
14	Bottom Solder	Solder Resist	0,010mm	3,5	
15	Bottom Overlay				

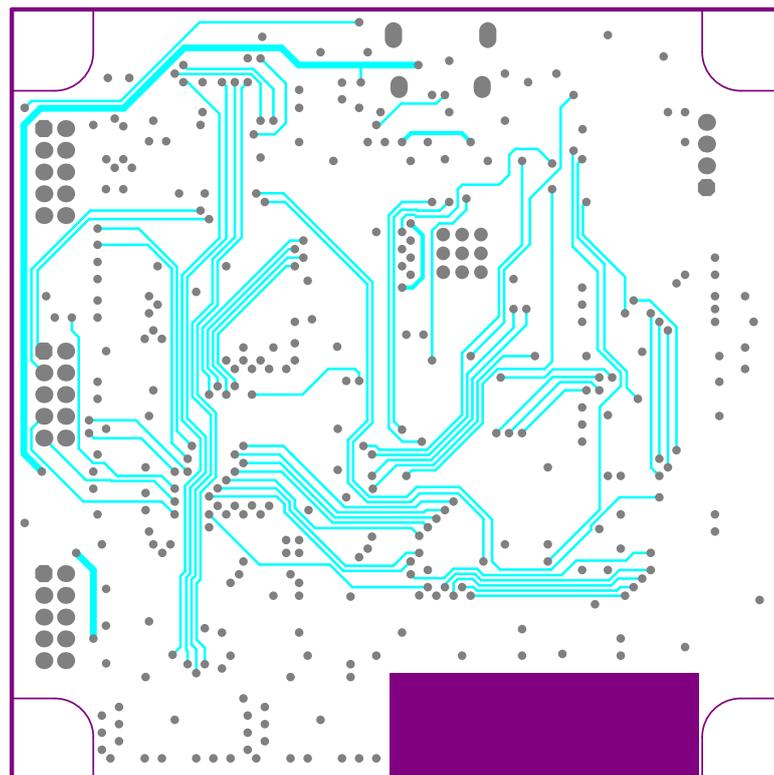


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Top Layer



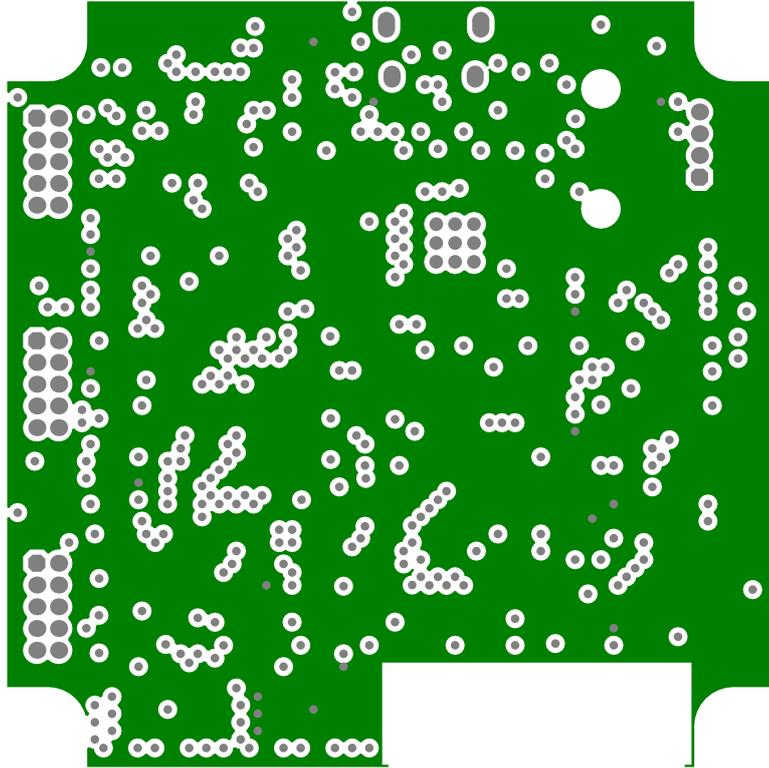
Signal Layer 1



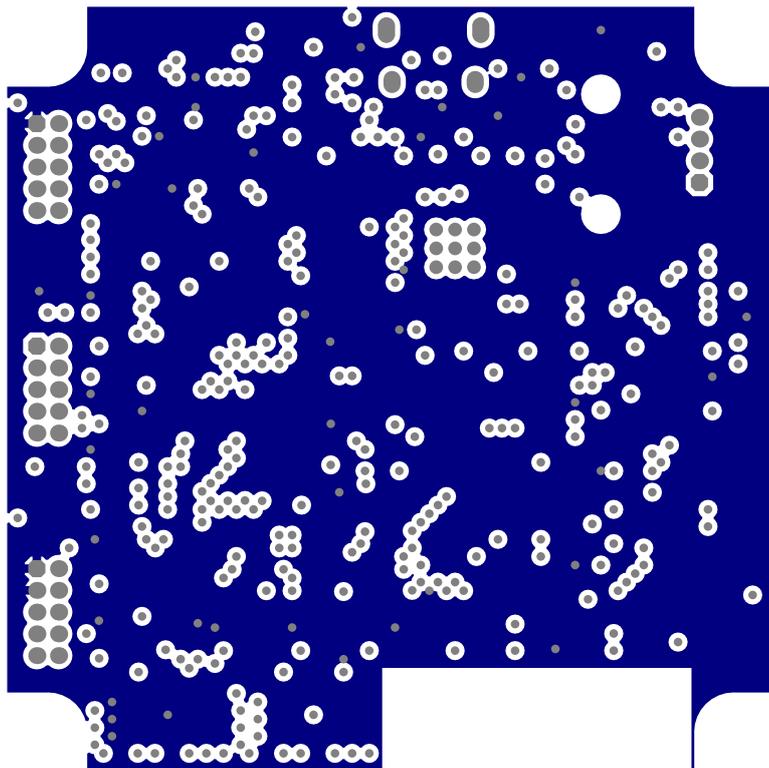


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1.18V



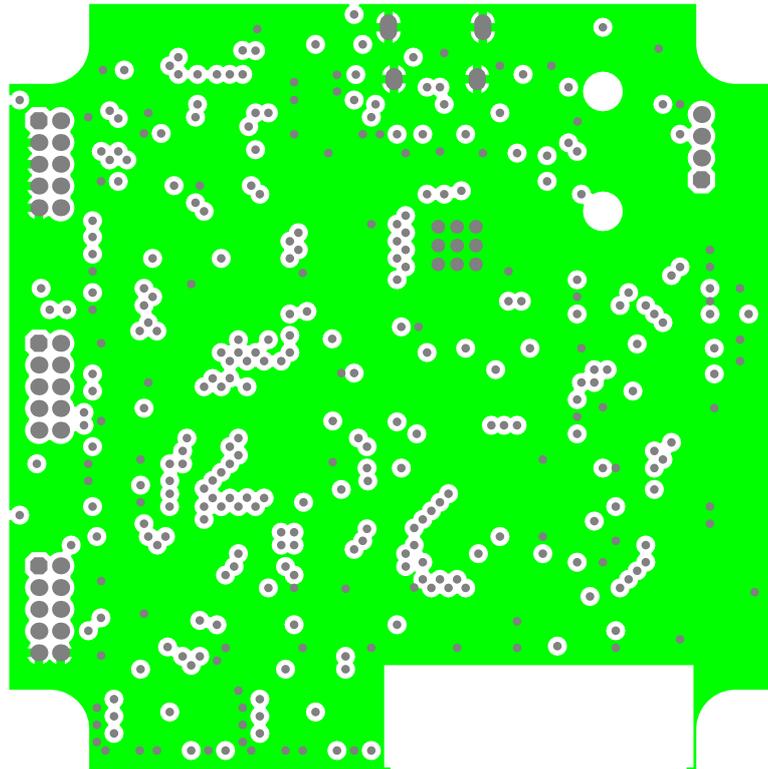
3.3V



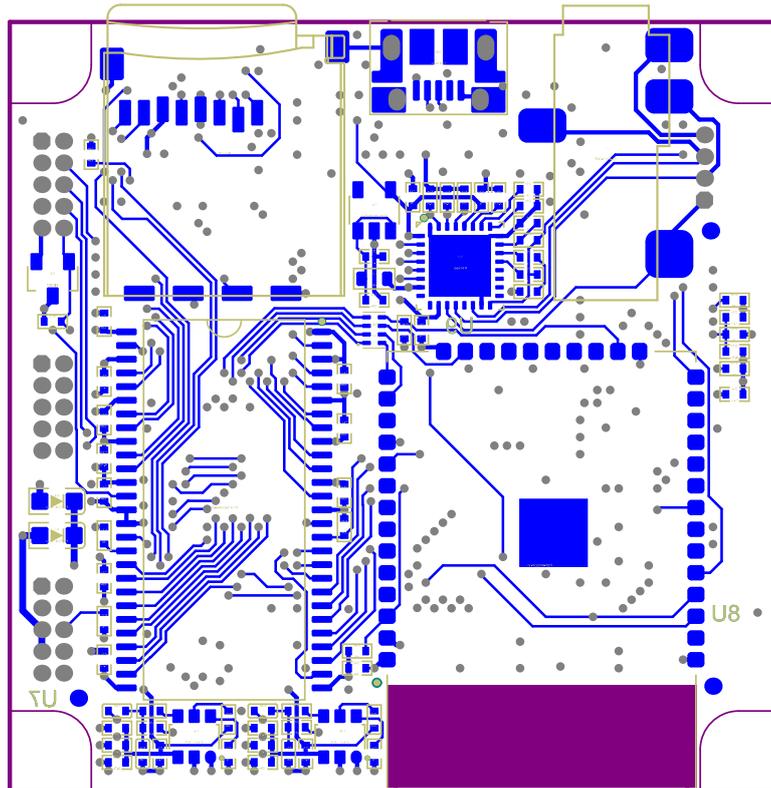


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Gnd



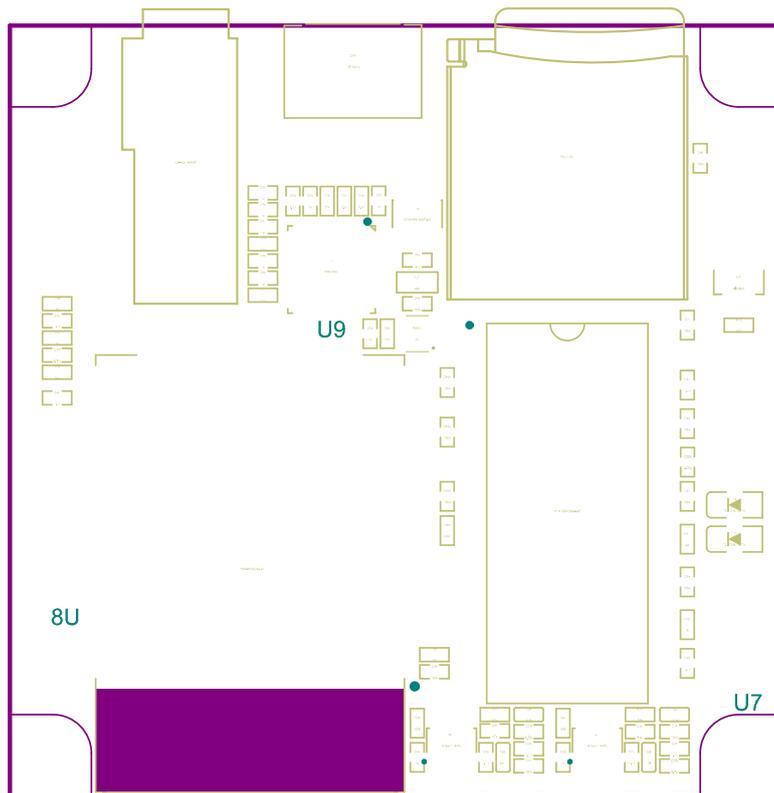
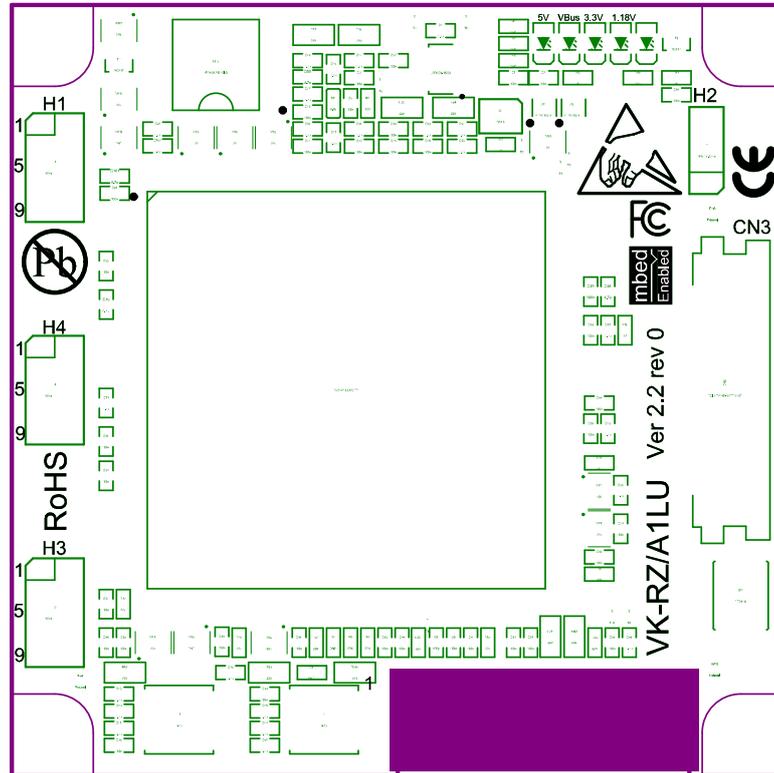
Bottom Layer





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14. Arrangement





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Revision overview list

Revision number	Description changes
1.0	Initial

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